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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,694	03/08/2004	Man-ho Chiang	3409-166	2864

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NIXON PEABODY, LLP
401 9TH STREET, NW
SUITE 900
WASHINGTON, DC 20004-2128

EXAMINER	
NGUYEN, HOA CAO	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,694	CHIANG ET AL.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-17* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 6/19/06 has been entered. Applicants have amended claim 3.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Bloom (US 5726615).

Regarding claim 1, as shown in figures 1 and 8, Bloom discloses an electromagnetic component formed from a multi-layer PCB comprising:

(a) A plurality of conductive traces 58 (flat electrical conductors, column 6, lines 57-58) having a curved shape (as shown in the figure) and two terminal ends (no number, as shown in the figure),

(b) each conductive trace formed on an insulating layer (no number, see column 6, lines 61-63) of the PCB and positioned such that the conductive traces form a stack (column 5, lines 21-26);

(c) a plurality of conductors (interconnecting vias - no number, column 7, lines 32-36) for interconnecting the terminal ends of each conductive trace to form at least one turn of a winding (figures 8A-C disclose multiple of turns);

(d) a first conductive layer 58a (considering the top layer as a first conductive layer - figure 8A as an example) attached to a first outer surface (see examiner remarks) of the PCB in a position at the top of the stack and having two terminal ends (each layer has two terminals, as shown in the figure) and approximately the same shape as the conductive traces;

(e) a first additional conductor (no number, shown in the figure - interconnecting via) for connecting at least one of the first conductive layer terminal ends to a terminal end of at least one of the conductive traces;

(f) a second conductive layer 58f (considering the bottom layer as a second conductive layer - figure 8A as an example) attached to a second outer surface (see examiner remarks) of the PCB in a position at the bottom of the stack and having two terminal ends and approximately the same shape as the conductive traces; and

(g) a second additional conductor (interconnecting via - no number) for connecting at least one of the second conductive layer terminal ends to a terminal end of at least one of the conductive traces.

Examiner remarks: It is noticed that the examiner picks figure 8A for an easy explanation purpose only, other figures are also incorporated in this Office Action.

Bloom discloses a structure, which is centered about a stack of flat conductive layers to form an inductor and/or transformed. As shown in column 7, line 18 continuing column 8, line 33, Bloom, discloses a double-sided PCB having one of the illustrated embodiments (fig. 8A-8C) formed within the PCB and interconnected to the circuit board circuit. The examiner considers the outer layers of the illustrated

embodiments that are formed on the outer surfaces of the PCB for electrical connection to the PCB's wiring patterns formed on its surfaces.

Regarding claim 2, as shown in figure 8A-8C, Bloom discloses a first one (58b) of the conductive traces, which is formed on the top surface of the PCB and a second one (58e) of the conductive traces is formed on the bottom surface of the PCB, and wherein the first conductive layer is in conductive contact (by interconnecting vias) with the top conductive trace and the second conductive layer is in conductive contact (by interconnecting vias) with the bottom conductive trace.

Regarding claim 4, Bloom discloses each the conductive layer is a metal foil (column 7, line 56-57).

Regarding claim 5, as shown in the figures, Bloom discloses each insulating layer, which defines an aperture 56 (column 6, line 59), wherein each conductive trace is in the shape of a loop positioned adjacent to the perimeter of a respective one of the apertures, and wherein the conductive layers are each shaped to define an aperture that corresponds to the shape of the apertures formed in the insulating layers, the component further comprising a core 44 (column 5, line 33) positioned in the space defined by the apertures. It is noticed that the conductive traces are insulating separated (column 6, lines 61-63) and each insulating layer must contain an aperture for sliding into the core 44.

Regarding claim 6, Bloom discloses the component, which is an inductor (column 3, line 20).

Regarding claims 7-10, as shown in the figures, Bloom discloses a plurality of winding turns formed by the conductive traces 58a-58h and the interconnecting vias (the conductors), and each winding turn is formed by at least 2 conductive traces.

Regarding claim 11, Bloom discloses every limitation as shown in claim 2 above including the electromagnetic component further comprising an insulator (no number, column 6, lines 61-63) disposed between the top conductive trace and the first conductive layer.

Regarding claim 12, Bloom discloses every limitation as shown in claim 5 above.

Regarding claims 13-15, Bloom discloses every limitation as shown in claims 7-10 above.

Regarding claim 16, Bloom discloses the plurality of conductors as interconnecting vias (see claim 1). Because plated conductive via is conventionally known, therefore Bloom anticipates the claim.

Regarding claim 17, Bloom discloses every limitation as shown in the claims 1-2 above.

Allowable Subject Matter

4. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Allowance

5. The following is an examiner's statement of reasons for allowance: The best prior art of record, Bloom (US 5726615), taken alone or in combination, fails to teach or fairly suggest the first conductive layer (58a, figures 8A-8C) and second conductive layer (58f/58h, figures 8A-8B/8C) are soldered directly onto the top and the bottom conductive trace (a stack of traces).

Response to Arguments

6. Applicant's arguments filed on 6/19/06 have been fully considered but they are not persuasive.

Remarks, claim 1, page 5 continuing page 6: The argument centers about the first and the second conductive layer 58a and 58f.

The Examiner firmly consider, at the final product of Bloom in its broadest means, that the layers 58a and 58f are attached to the outer surfaces of the circuit board, wherein the circuit board is defined as a multilayer circuit board having any other layers excluding the layers 58a and 58f. Applicants should be noted that in interpreting a multilayer circuit board, any stack of layers could be considered as a circuit board and any layer outside the predefined circuit board is properly considered as attached to the surfaces of the circuit board.

Remarks, claim 1, page 6 and 7: The argument centers about the first and the second conductive layer 58a and 58f are formed on an insulating layer.

The Examiner agrees. However, claim 1 does not contain any limitation that requires the first and the second conductive layer attached directly onto the stack of conductive traces without an insulating layer in between.

Remarks, claim 2, page 8: The argument centers about the first and second conductive trace, which is formed on an insulating layer.

The Examiner firmly considers, at the final product of Bloom in its broadest means, that layer 58e and 58f are formed on an insulating layer (see Bloom, col.6:61-63, col.7:1-9 and col.8:17-19).

Remarks, claim 4, page 8: The argument centers about the conductive layers and insulating layer.

Claim 4 does not have any limitation regarding the insulating layer but a metal foil.

Remarks, claim 11: The argument centers about Bloom does not disclose an insulator between a top conductive trace and a first conductive layer.

The argument is not persuasive. There is an insulator layer in between layers 58a and 58b (see Bloom, col.6:61-63).

Remarks, claim 17: Same argument as above.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen
8/30/06

KAMMIE CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800